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Stability of amorphous InGaZnO thin film transistors with a bottom gate structure

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Introduction

Amorphous oxide semiconductors (AOSs) are emerging as promising materials for the active layers of thin film transistors (TFTs), which are used in active-matrix liquid crystal display (AMLCD) and active-matrix organic light-emitting diode display (AMOLED). This is largely due to the high field-effect mobility, excellent uniformity and low-temperature processing of AOSs, compared to conventional amorphous silicon.[1,2] For the practical use of AOS-based TFTs, however, some critical issues such as stability need to be solved.

In this work, we have investigated the stability of TFTs based on *a*-InGaZnO films in detail. A shallow trap model is proposed to explain the large threshold voltage shifts of as-prepared devices. It is found that shallow traps may exist in as-deposited *a*-IGZO films, which are not compact. The shallow traps can be annealed out to improve the device stability.

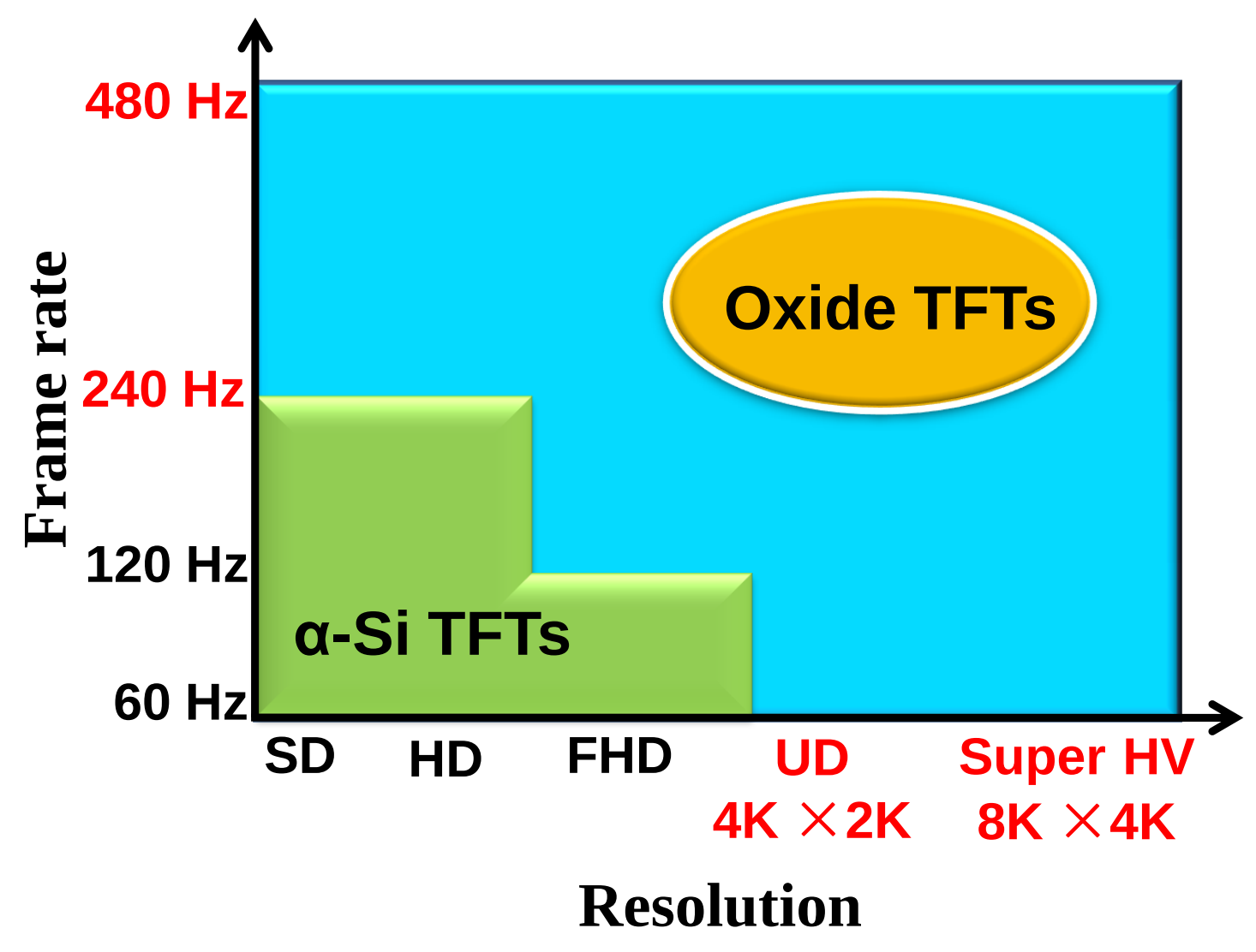

Fig. 1. TFT innovation for flat panel displays

Experimental

The channel layer deposition:

- ➢ Via PLD (10Hz; 300 mJ)
- ➢ Ceramic target
- ➢ Room temperature
- ➢ Oxygen partial pressure: 6.7 Pa
- ➢ Substrate-target distance: 4.5 ~ 6 cm
- ➢ Thickness: 50 nm
- ➢ Annealing at 400 ℃ in air

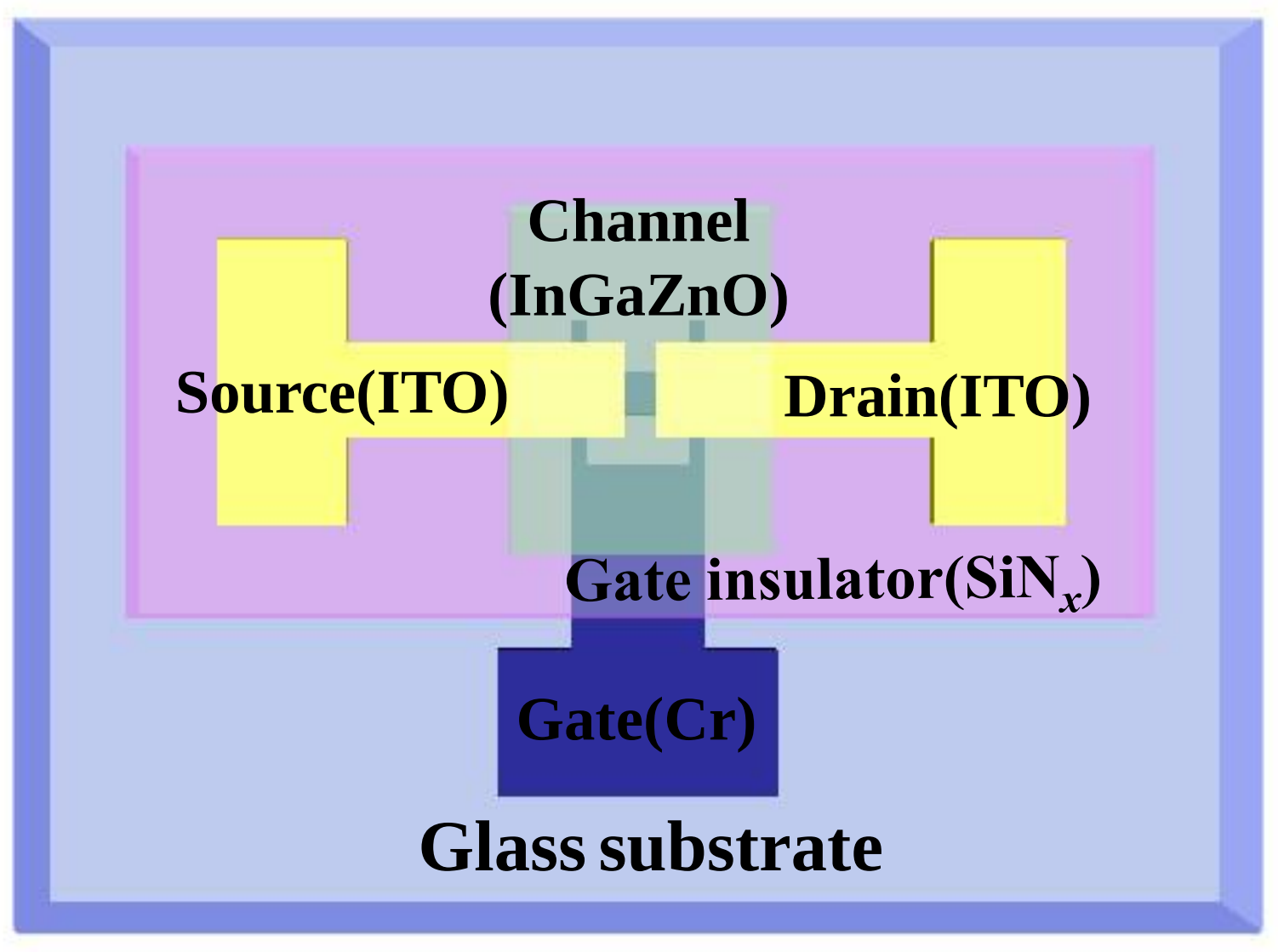

Fig. 2. Schematic of an *a*-InGaZnO TFT in a bottom-gate coplanar configuration. [3]

Results and discussion

A. Stability of as-prepared *a*-InGaZnO TFTs

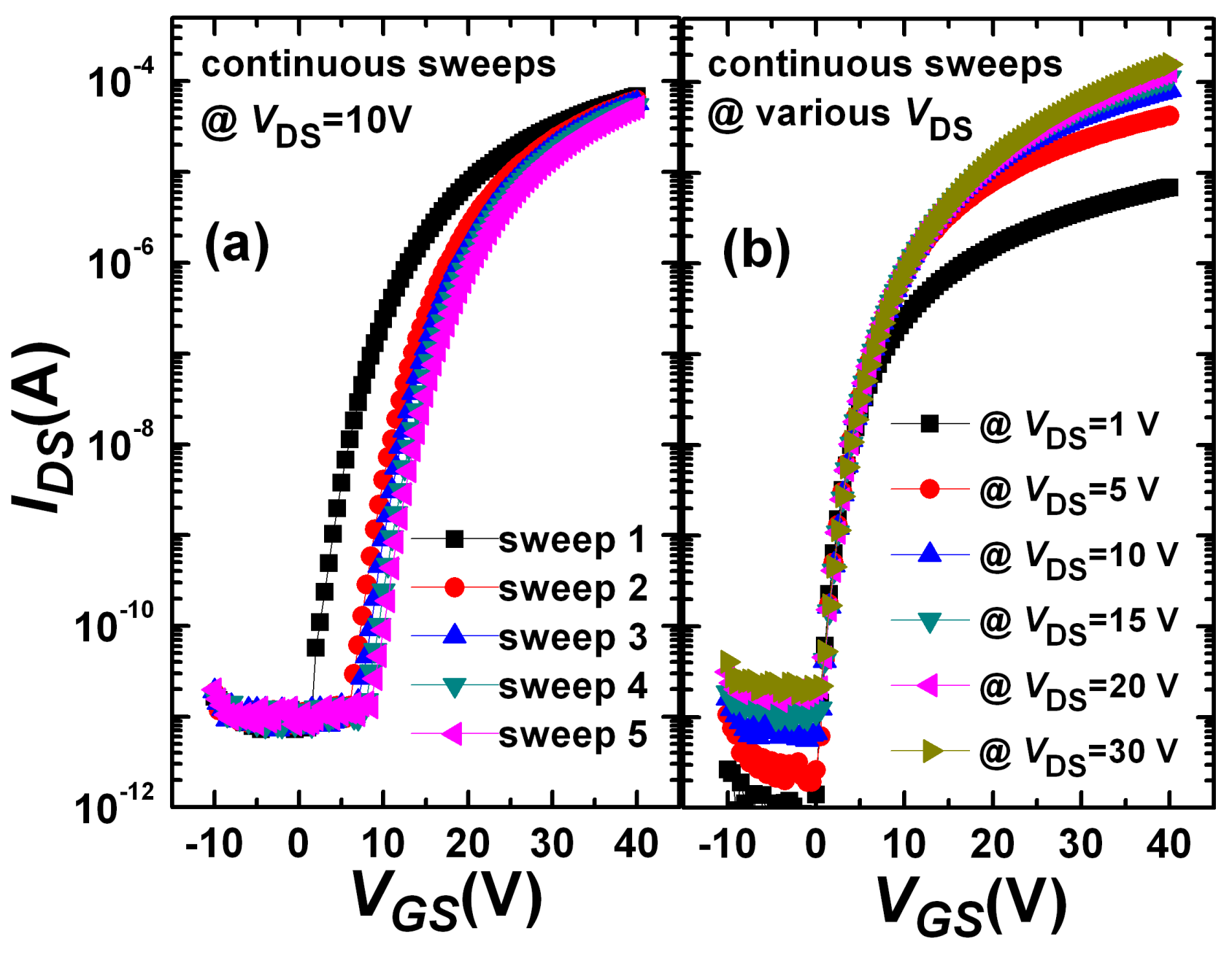

Fig. 3. Transfer curves of (a) an as-prepared *a*-InGaZnO TFT under continuous gate voltage sweeping for five times at a sweep rate of 0.2 V/s and (b) the annealed *a*-InGaZnO TFT under continuous gate voltage sweeping with V_{DS} varying from 1 to 30 V.

☐ A large ΔV_{th} of ~ 5V after the first sweep for the as-prepared *a*-InGaZnO TFT .

☐ No obvious change in the V_{th} is observed in the annealed device.

A shallow trap model

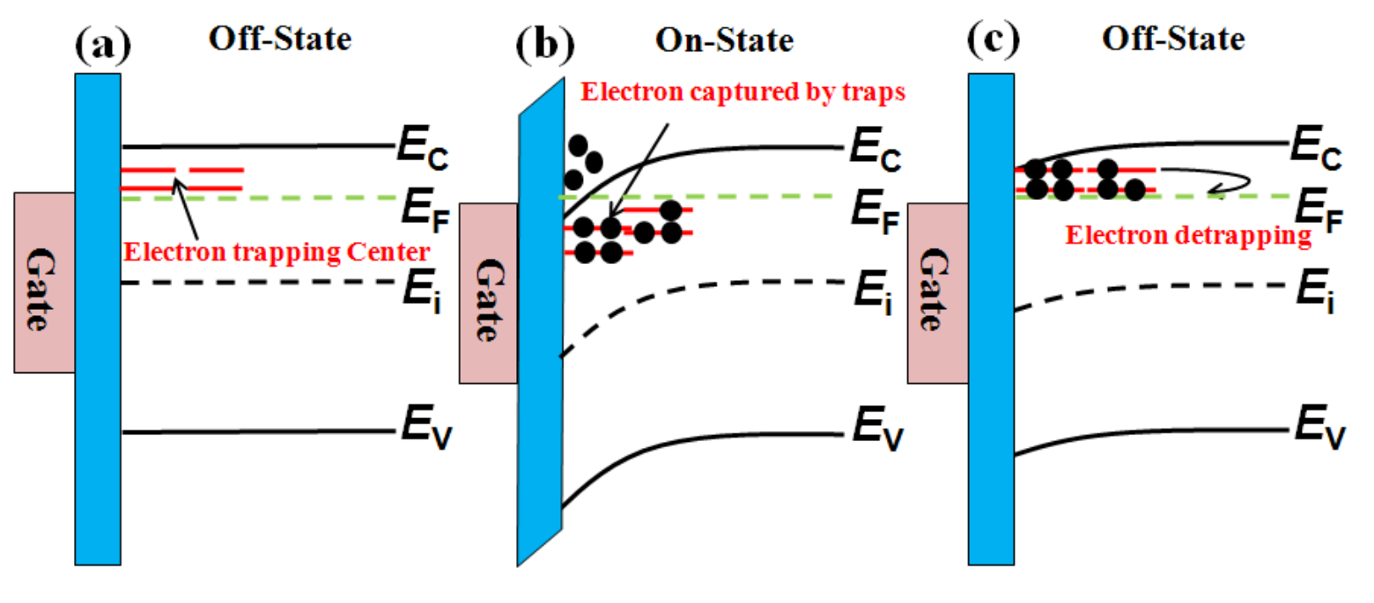

Fig. 4. Energy band diagrams of *a*-InGaZnO TFTs. (a) Off-state before applying gate voltage. There are some shallow defects which act as electron trapping centers in as-deposited *a*-IGZO films. (b) On-state at the first sweep. Most of the traps are quickly filled with electrons. (c) Off-state after the first sweep. the trapped electrons hop to a low energy level by relaxation.

What are these shallow defects???

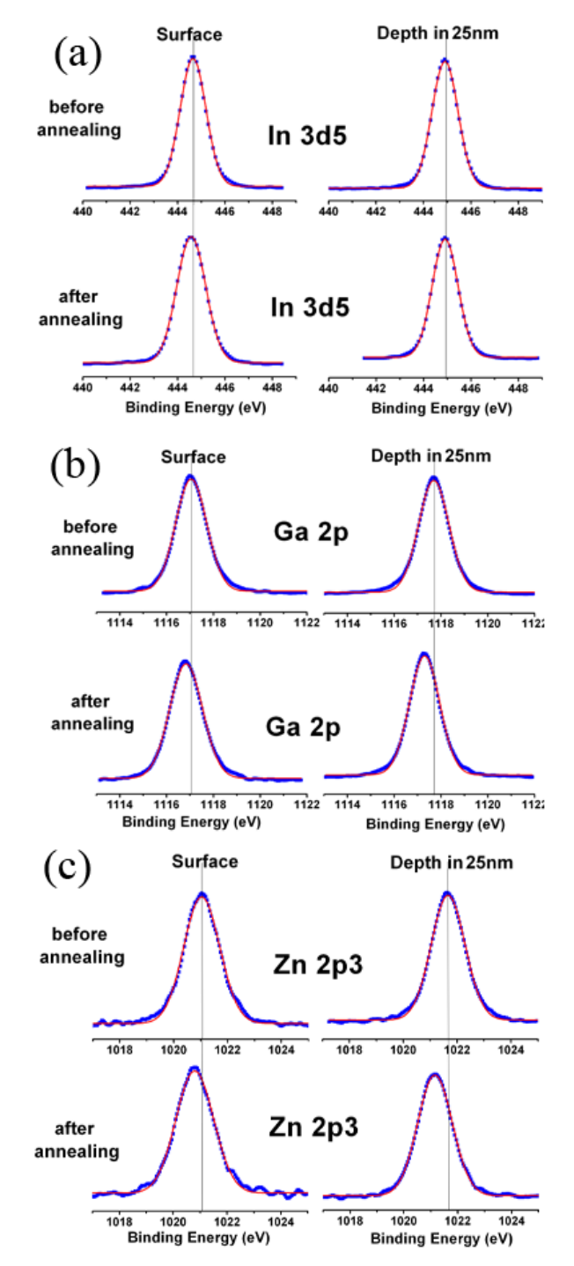

Fig. 5. XPS spectra of (a) In $3d_{5/2}$, (b) Ga $2p_{3/2}$ and (c) Zn $2p_{3/2}$ of the as-deposited and annealed *a*-IGZO films with a thickness of 50 nm.

	element	C1s	In3ds	Ga2p	Zn2p3
Surface	Before annealing	284.80 eV	444.7 eV	1117 eV	1021.05 eV
	After annealing	284.80 eV	444.6 eV	1116.8 eV	1020.8 eV
Depth in 25nm	Before annealing	284.80 eV	444.90 eV	1117.69 eV	1021.67 eV
	After annealing	284.77 eV	444.90 eV	1117.29 eV	1021.16 eV

Table 1 Binding energies of C 1s, In 3ds, Ga 2p and Zn 2p3 in *a*-IGZO films at the surface and in the bulk with a depth of 25 nm.

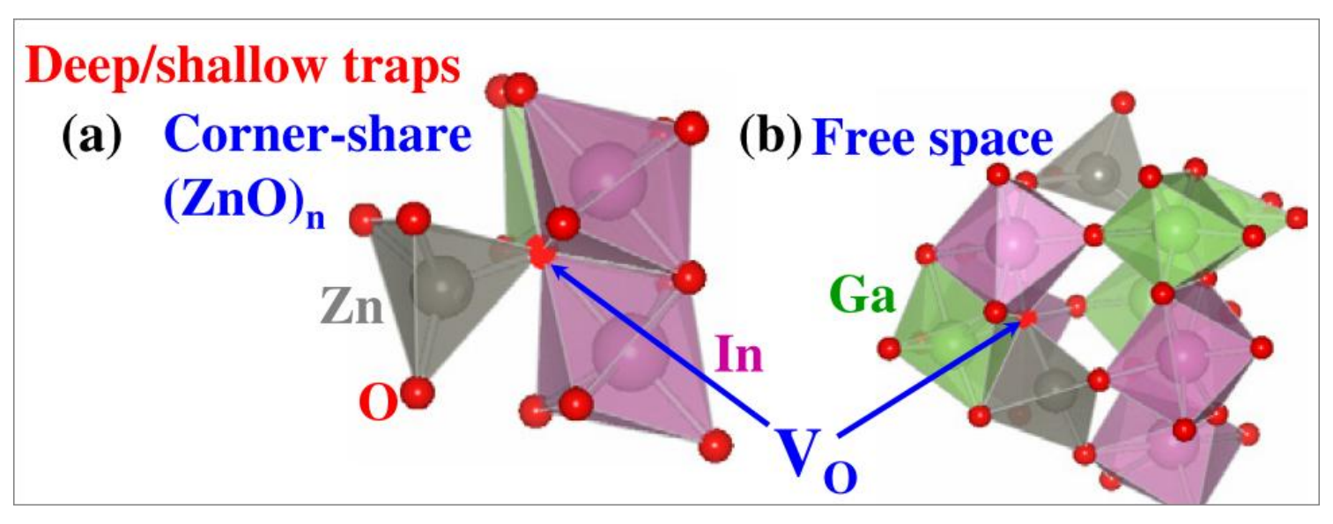

Fig. 6. Local coordination of oxygen vacancies[4]

☐ The binding energies of Zn^{2+} and Ga^{3+} downshift by 0.2 ~ 0.5 eV after annealing

☐ The structure of as-deposited *a*-IGZO films is not compact.

☐ Shallow traps may be related to weak chemical bonds of Zn-O and Ga-O.

B. Stability of annealed *a*-InGaZnO TFTs

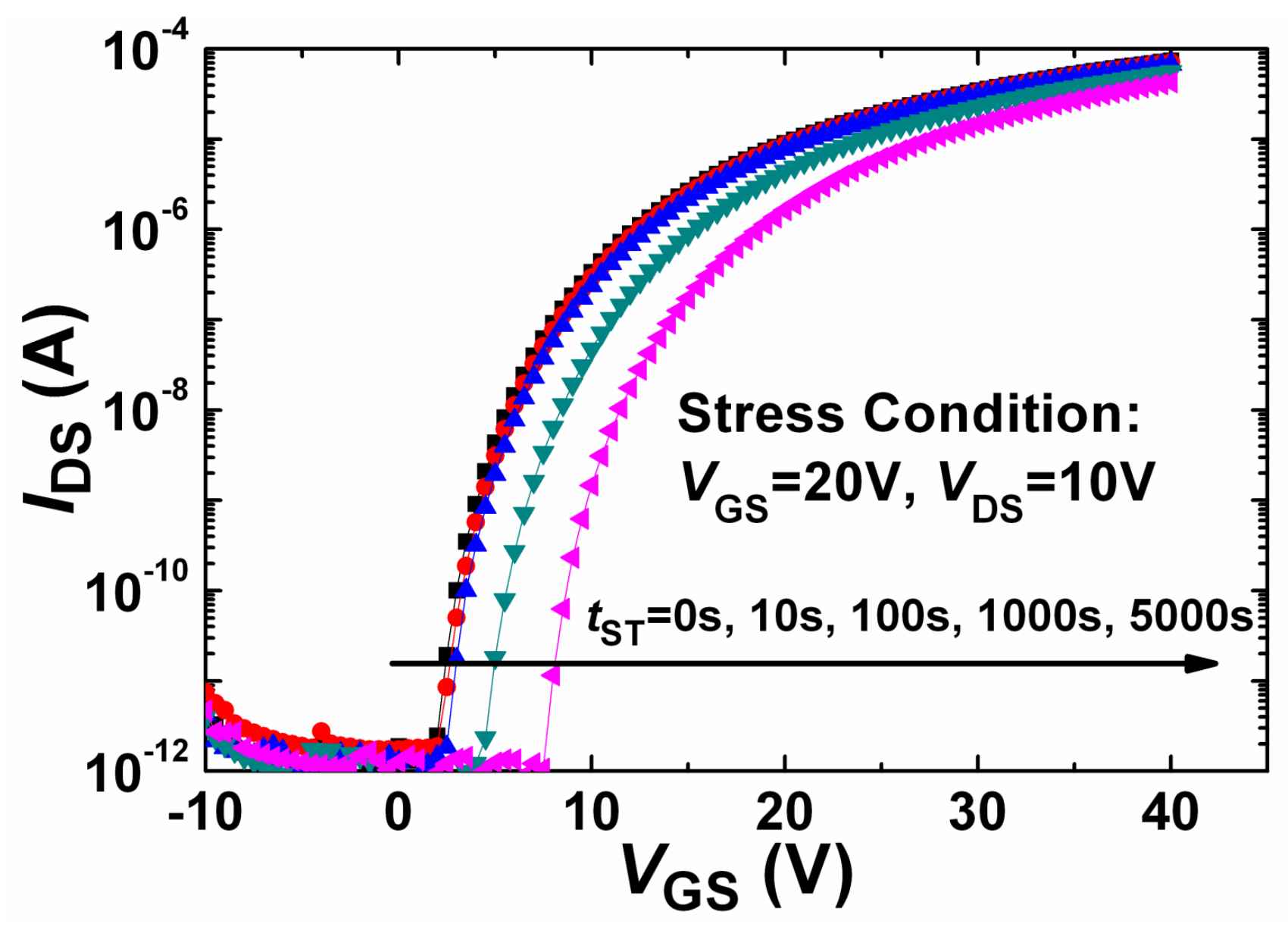

Fig. 7. Transfer curves of an annealed device at a fixed drain voltage of 10 V and a fixed gate voltage of 20 V. The stress time varies from 0 to 5000 s. The source electrode was grounded.

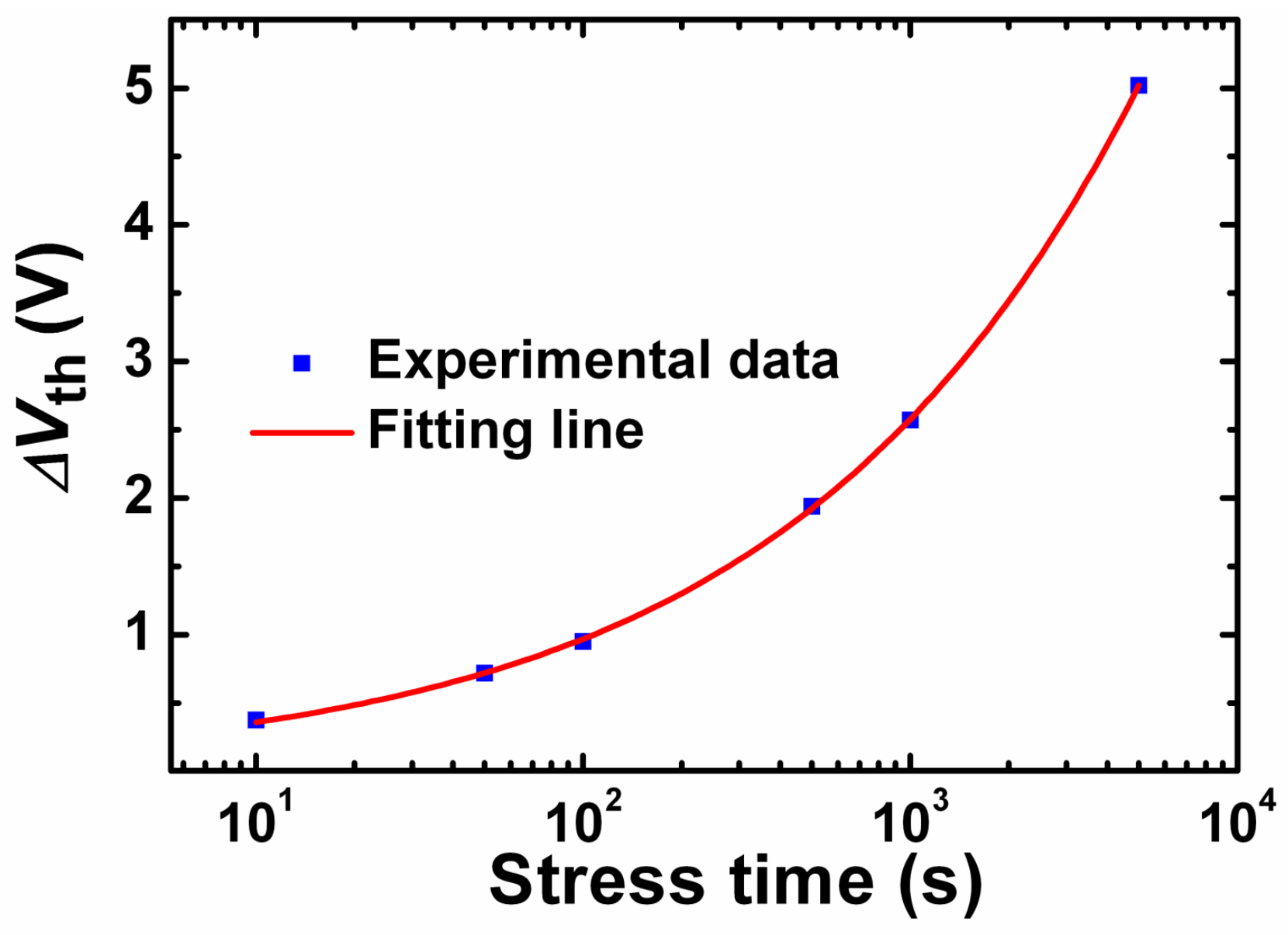

Fig. 8. Dependence of ΔV_{th} on stresss time. The data are well fitted by use of a stretched-exponential equation with a characteristic trapping time of 6×10^5 s and a stretched-exponential exponent of 0.43.

☐ Positive V_{th} shifts without significant change of sub-threshold slope

☐ Charge trapping at the interface

☐ Stretched-exponential equation:

$$\Delta V_{th} = \Delta V_{th0}\left\{1-\exp[-(t/\tau)^{\beta}]\right\}$$

Conclusions

◆ During the gate voltage sweeping of as-prepared devices there is a large ΔV_{th}, which may be due to the shallow traps induced by weak chemical bonds of Zn-O and Ga-O.

◆ The stability of devices is improved after annealing. The change of threshold voltage with stress time is attributed to a charge-trapping mechanism.

References

1. K. Nomura, H. Ohta, et al. *Nature* **432**, 488 (2004).
2. J. C. Park, S. Kim, et al. *Adv. Mater.* **22**, 5512 (2010).
3. J. Zhang, X. F. Li, J. G. Lu, Z. Z. Ye, et al. *J. Appl. Phys.* **110**, 084509 (2011).
4. T. Kamiya, K. Nomura, et al. *Sci. Technol. Adv. Mat.* **11**, 044305 (2010).

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